IN THE CLAIMS

1. (Currently amended) A thin film transistor array panel comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating layer covering the gate electrode and the substrate;

a source electrode and a drain electrode formed on the gate insulating layer;

a semiconductor layer formed on the gate insulating layer and the source electrode and the drain electrode ; and

a passivation layer covering the semiconductor layer, the source electrode, the drain electrode, and the gate insulating layer, wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C or Parylene D.

2. (Previously presented) The thin film transistor array panel of claim 1, wherein the substrate is made of one material selected from plastic, glass, and metal.

3. (Canceled)

4. (Original) The thin film transistor array panel of claim 1 further comprising a pixel electrode formed on the passivation layer and connected to the drain electrode through a contact hole of the passivation layer that exposes a portion of the drain electrode.

5. (Currently amended) A manufacturing method of a thin film transistor array panel comprising:

forming a gate electrode on a substrate;

forming a gate insulating layer covering the gate electrode on the substrate;

forming a source electrode and a drain electrode on the gate insulating layer;

forming a semiconductor layer covering the source electrode and a portion of the drain electrode; and

forming a passivation layer covering the gate insulating layer, the source electrode, the drain electrode, and the semiconductor layer, wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

6. (Previously presented) The manufacturing method of a thin film transistor of claim 5, wherein the gate insulating layer and the passivation layer is made of Parylene by chemical vapor deposition.

7. (Currently amended) A thin film transistor comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating layer covering the substrate and the gate electrode;

a semiconductor layer formed on the gate insulating layer and disposed on the corresponding portion of the gate electrode;

a source electrode and a drain electrode contacting portions of the semiconductor layer, formed on the gate insulating layer, and separated by a predetermined distance; and

a passivation layer covering the semiconductor layer, the gate insulating layer, the source electrode, and the drain electrode, wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

8. (Currently amended) A thin film transistor array panel comprising:

a substrate;

a source electrode and a drain electrode formed on the substrate and separated by a predetermined distance;

a semiconductor layer covering the source electrode and the drain electrode;

a gate insulating layer covering the substrate and the semiconductor layer;

a gate electrode formed on the gate insulating layer and disposed on the corresponding portion between the source electrode and the drain electrode; and

a passivation layer covering the gate insulating layer and the gate electrode, wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

9. (Original) The thin film transistor of claim 8 further comprising a pixel electrode formed on the passivation layer and connected to the drain electrode through a contact hole of the gate insulating layer and the passivation layer that exposes a portion of the drain electrode.